PR2530 8x 4:1 MUX

Eight 4:1 multiplexers with serial interface and LNA

PR2530 contains eight 4:1 mulitplexers in one chip. By connecting several chips in series, the number of channels can be further increased.
The main application is for the receiving part of imaging ultrasound instruments.
In addition to the multiplexer, it contains a low-noise amplifier for each channel, to drive the load of a cable with parasitic capacitance.

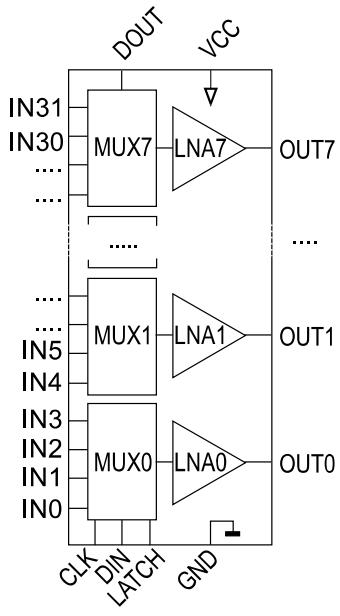
FEATURES

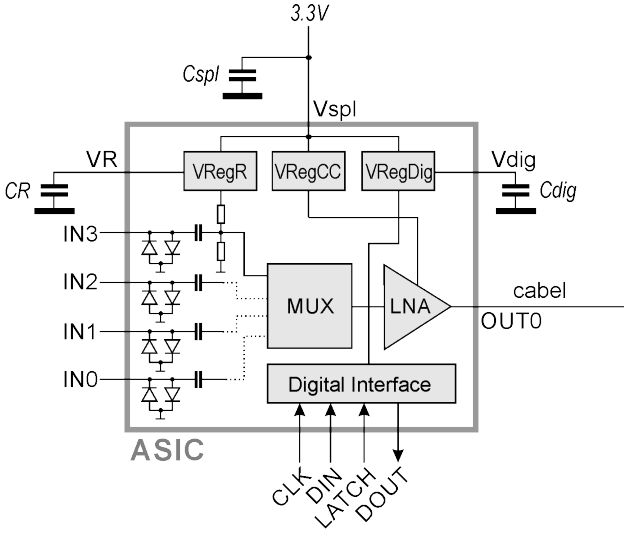
- 8 channels with 4:1 multiplexers
- independently switchable inputs, allowing to group several inputs to one output
- cascadable serial interface
- AC coupled input
- output buffered by LNA
- supply voltage 3.3V

APPLICATIONS

- Imaging ultrasound systems

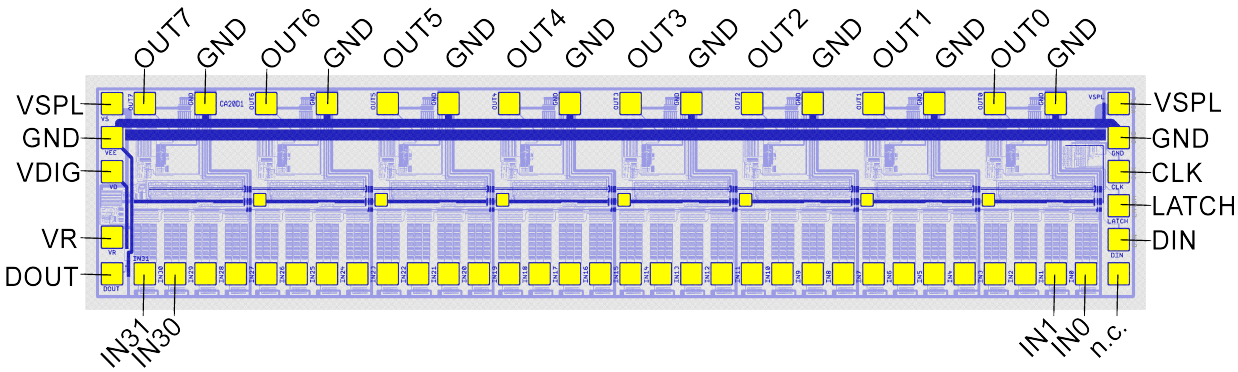
BLOCK DIAGRAM



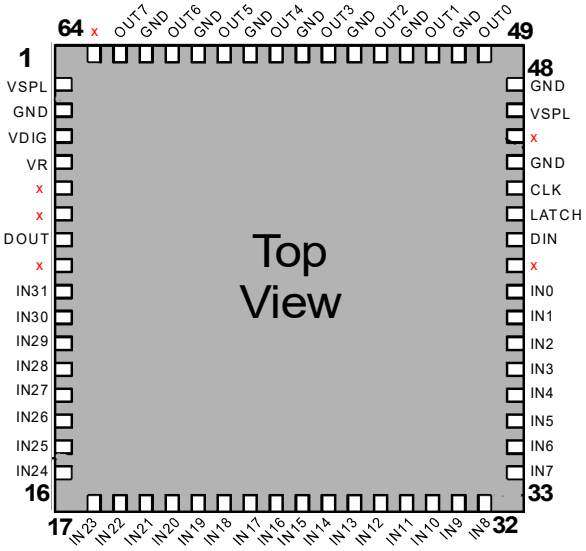


Left: diagram of whole chip

Right: detailed diagram of one 4:1 MUX



PIN DESCRIPTION

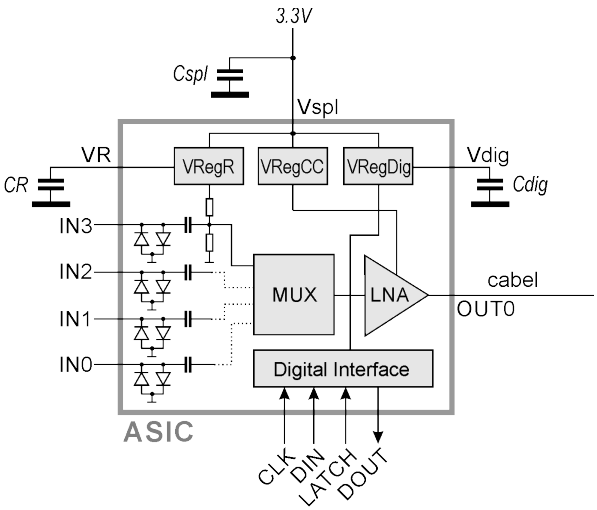


Pin No	Pin Name	Pin Function Description
1	VSPL	supply voltage
2	Gnd	ground connection
3	VDIG	connection to reservoir cap

Pin No	Pin Name	Pin Function Description
		for digital supply
4	VR	connection to reservoir cap for reference voltage
5-6	n.c.	no connection
7	DOUT	output of shift register
8	n.c.	no connection
9-40	IN31 ... IN0	input channel 31 ... 0
41	n.c.	no connection
42	DIN	serial register data input
43	LATCH	serial register data latch
44	CLK	serial register data clock
45	GND	ground connection
46	n.c.	no connection
47	VSPL	supply voltg (connect with pin 1)
48-63	GND	ground connection
49-64	OUT0 ... OUT7	output from LNAs

Properties

BLOCK DIAGRAM



Each block (4 inputs, 1 output) contains
- an input limiter, clamping the signal to ±0.7V
- a coupling capacitor and following DC bias source
- a 4:1 multiplexer, controlled by the digital interface
- a low-noise amplifier

The circuit blocks are supplied from the 3.3V power supply via internal voltage regulators. To smoothen the voltage, a reservoir capacitor should be connected to Vspl, VR and Vdig. This prevents e.g. a distortion of the reference voltage by the pulsing digital supply signal.

ELECTRICAL CHARACTERISTICS

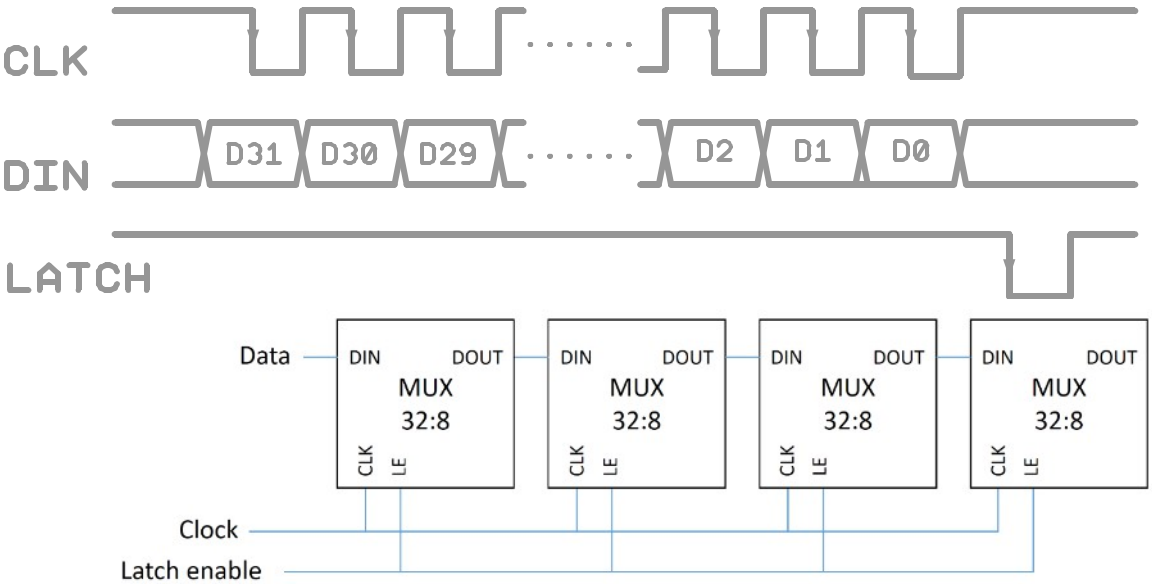
Ta = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{SPL}	Supply voltage		3.0	3.3	3.6	V
I_{SPL}	Supply current				20	mA
V_{clamp}	Input clamping voltage		-0.7		0.7	V
I_{in}	Input current				0.5	mA
	DC voltage level after coupling capacitor		1.14	1.20	1.26	V
	DC offset between channels within one group of 4		-1%		+1%	
	DC offset between channels of different groups		-2%		2%	
Z_{inp}	Input impedance		100			kΩ
	Attenuation input > MUX out	switch open	60			dB
	Attenuation input > MUX out	switch closed			1*	dB
	Transmitted signal frequency		1		6	MHz
	Attenuation between adjacent channels		60			dB
Ta	Ambient temperature		0		60	°C

* The attenuation with closed switch depends on the frequency and parasitic input resistances and capacitances.

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Units
	Logic Input High Level (DIN, CLK, LATCH)	1.0		6.0	V
	Logic Input Low Level (DIN, CLK, LATCH)	0		0.4	V
	Logic Input Capacitance (DIN, CLK, LATCH)			10	pF
	Logic Output High Level (DOUT) @ I_{out} = 50µA	V_{spl} - 0.2		V_{spl}	V
	Logic Output Low Level (DOUT) @ I_{out} = 50µA	0		0.2	V
	Logic Output Current (DOUT)	0.1			mA
	Clock Period		50		ns
	Clock High Time		25		ns
	Clock Low Time		25		ns
	Data Setup Time		10		ns
	Data Hold Time		5		ns
	Clock to Latch Time	75			ns
	Latch High Time	50			ns

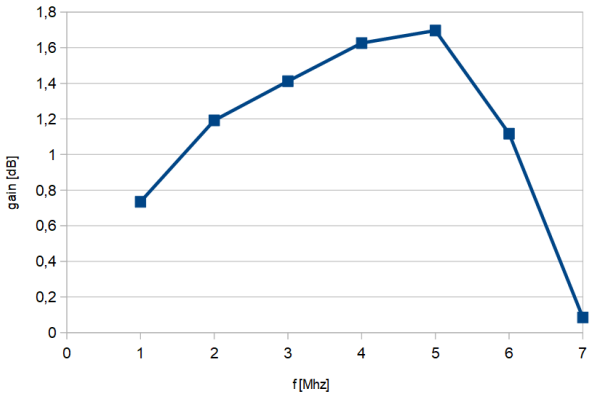


LNA

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Output voltage	Vin = 0	1.14	1.20	1.26	V
	Output voltage range		0.1		2.0	V
	Frequency range		1		5	MHz
	Output impedance	@ 3 MHz			20	Ohm
	Load resistance connected to output		500			Ohm
	Load capacitance connected to output				100	pF
	Gain			±10		dB

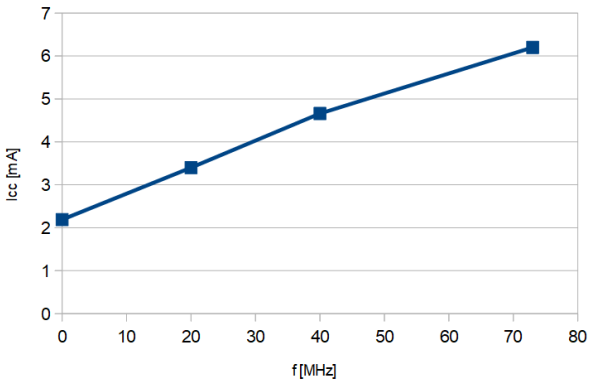
Performance

TRANSFER FUNCTION



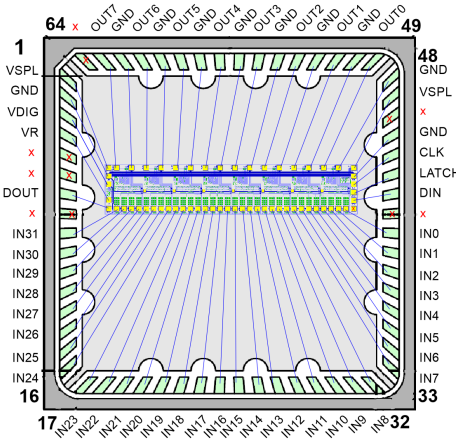
The transfer function is limited by the AC coupling at low frequencies, and by the LNA at high frequencies.

SUPPLY CURRENT FOR SHIFT REGISTER



Digital supply current vs. clock frequeny of shift register

Package Dimensions



Package: QFN 9.0 x 9.0
All parts are RoHS compliant. Finish is pure tin.
Detailed package information on request.

This integrated circuit has been developed as part of the joint research project "ULTRAWEAR" (Ultrasound-based Wearable as biofeedback system for effective muscle training in chronic dorsal pain).
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Bundesministerium für Bildung und Forschung

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