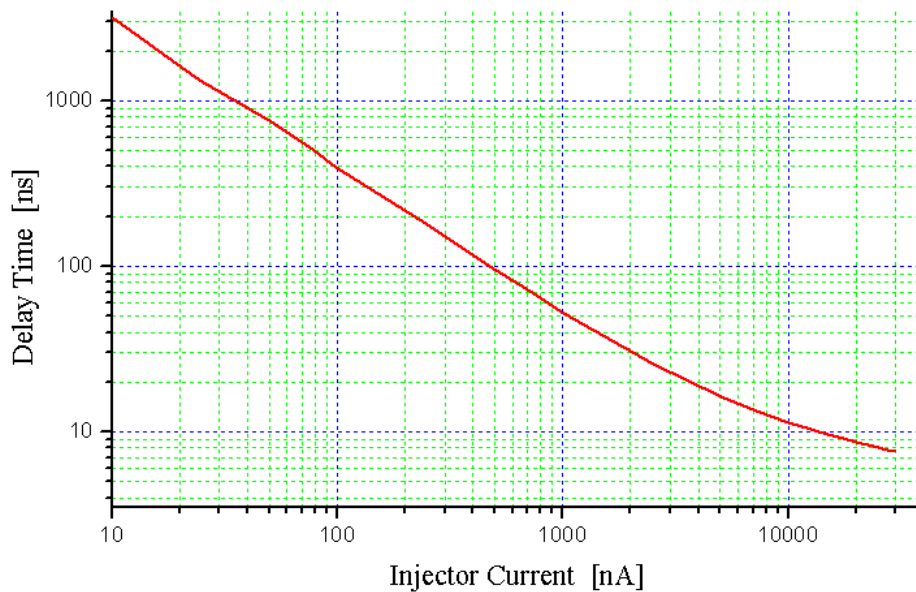


CCL GATES

ModuS U6 process allows the integration of special logic gates in the CCL technique (constant current logic). A vertical injector structure is used, thus providing a high gate current gain at lowest currents. The very compact structure allows integration densities of more than 1000 gates per square millimeter and more including wiring, depending on the application.

The signal propagation time of the gate depends on the value of the injector current, as shown in the following diagram.



Propagation delay t_{PD} as a function of the injector current

The CCL technology has the advantage that the gate delay times can be adapted to the demanded frequencies by changing the injector current. Thus the power dissipation is minimized ($1\mu\text{W}/\text{gate}/\text{MHz}$ at 1V supply voltage). Each block can be operated at an optimized current level, i.e. blocks running at high clock frequencies are biased with a higher injector current than slow blocks. A simple ring oscillator can be used as a current controlled oscillator.