High Voltage Complementary Epi Free LDMOS Module with 70 V PLDMOS for a 0.25 μm SiGe:C BiCMOS Platform

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Abstract — **We demonstrate the integration of a low-cost, high-voltage complementary LDMOS module with BVdss of -71V and 83V for the PLDMOS and the NLDMOS, respectively, into an advanced industrial 0.25 μm SiGe:C BICMOS process. The essential deep N-well for the high voltage PLDMOS is formed by a single 6 MeV P implantation step. BVdss*ft of the NLDMOS accomplishes record values > 900 VGHz.**

Index Terms — **Silicon RF-LDMOS technology, LDMOS, power devices, CMOS analog integrated circuits**

I. INTRODUCTION

LDMOS transistors are widely used for RF power amplifiers for wireless applications because of their excellent electrical parameters such as gain, efficiency, linearity, reliability and low cost. Key challenges at integration of LDMOS transistors into a highly scaled CMOS process with a thin gate oxide are good RF performance, high break down voltage and low on-resistance at acceptable device degradation.

State of the art fully integrated, high performance power management devices require complementary high voltage transistors in the power amplifier output stage working at switching frequencies of several MHz. A sufficient RF performance is essential to meet the requirements for a pulse rising time in ns range. The integration of RF LDMOS transistors with high voltage capability enables dc/dc converter designs with high switching frequencies up to several 10 MHz. The advantages of a high switching frequency are significantly reduced values for the input and output capacitances and the output inductance at high conversion efficiency. The integration of the inductor into the package of the dc/dc converter, dramatically reduces pc-board real-estate, lowers cost, and increases system performance.

The modular cost effective integration of complementary RF LDMOS transistors [1,2] and devices with high blocking voltage for 42 V Vdd operation into IHP's industrial 0.25 μm CMOS/SiGe:C BiCMOS technology platform [3] addresses besides power management, also markets including RF power amplifiers, class D audio amplifiers, MEMs drivers, display drivers and automotive applications for the next generation 42 V automotive power net. A 0.25 μm base CMOS platform technology enables a cost effective modular integration of large memory blocks, essential for performance digital building blocks for SOC solutions.

In [4] the integration of a 60 V PLDMOS into a CMOS technology (thick gate oxide, Vgs = 15 V, LOCOS isolation, 1 μm design rules) is described, which makes use of an epitaxially grown n-well and enables BVdss of 60 V. The authors in [5] describe a 55 V PLDMOS integrated into a 0.18 μm CMOS platform, using a pocket implant to suppress leakage and device parameter roll off. High energy P implantation is used to isolate the devices from the p-substrate.

II. TECHNOLOGY

In this work we give an approach to integrate complementary high voltage LDMOS transistors into a qualified 0.25 μm SiGe:C BiCMOS technology (Figs. 1, 2) with a gate oxide thickness of 5 nm corresponding to a gate voltage of ±2.5 V. In Fig. 3 the scheme of the process flow is illustrated. The full process results from the optional integration of the SiGe:C HBT module, the low voltage RF-LDMOS module and the HV-LDMOS module into a base 0.25 μm RF-CMOS flow. Any module integration must not change the CMOS device parameters in order to maintain the reuse of available design libraries.

A deep low dose 6 MeV P implantation performed immediately after implantation of the standard CMOS wells forms the high voltage n-well for the PLDMOS. The implantation energy of 6 MeV was given as a fixed boundary condition for process integration. The standard p- and n-wells overlap the gate over a length of LIT,

forming the gate lengths of the inside NMOS and PMOS transistors. The LDD regions were implanted before gate structuring. The connection of the channel to the drift region is strongly affected by LCC. 2D process and device simulation was performed using the DIOS/DESSIS simulator to obtain a maximum break down voltage BVdss at a minimum on-resistance Ron. The position and the parameters of the LDD implantations were carefully tuned to ensure a sufficient channel connection near the gate overlapped trench edge and a fully depletion in the "off state" inside the drift space beneath the shallow trench. A properly designed contour of the LDDs outside the drain region prevents from a lateral drain to substrate breakdown. Figs. 4 and 5 show the simulated doping contour maps for the NLDMOS and the PLDMOS, respectively.

III. DEVICE RESULTS

The primary electrical parameters of the new devices are summarized in Table 1. Fig. 6 shows BVdss as function of drift length Ld. A desired value for BVdss can be obtained by adjusting the drift length Ld. BVdss for the PLDMOS is limited by the vertical breakdown of the drain to HV-n-well pn-junction. For the PLDMOS (Ld = 5 µm) the measured value for BVdss of –73 V corresponds well with the simulation result of -70 V. Typical measured breakdown, transfer and output characteristics of 5.6 µm wide devices with a drift length Ld=3 µm are shown in Figs. 7, 8 and 9. The small shift in the subthreshold curves in linear and saturation operation mode (Fig. 8) and the low leakage current up to the onset of break down (Fig. 7) demonstrate that both NLDMOS and PLDMOS are far from gate break down or punchtrough. Fig. 10 illustrates the RF performance of the devices. Note, that for the PLDMOS RF S-parameter measurements were available only for the device with Ld = 5 µm. Fig. 11 proves the good long term drift stability of both transistors. For 42 V Vdd operation a drift for both Idlin, which corresponds to Ron, and Idsat < 10% within 20 years operation lifetime can be predicted.

IV. SUMMARY AND CONCLUSIONS

In summary, we have demonstrated a cost effective modular integration of high voltage complementary LDMOS transistors with record parameters suitable for smart power (Vdd=42 V) and RF applications into a state of the art industrial 0.25 µm CMOS platform. Our primary results can be summarized as follows: (1) BVdss/Ron values obtained: -71 V/205 mΩmm^2 for PLDMOS and 83 V/60 mΩmm^2, 103V/236 mΩmm^2 for NLDMOS. (2) Excellent DC characteristics. (3) RF performance with maximum values for ft/fmax 2.7 GHz/8.6 GHz (BVdss = -71 V) for PLDMOS and 11 GHz/41 GHz (BVdss = 83 V), 9 GHz/29 GHz (BVdss = 103 V) for NLDMOS. (4) HV-NLDMOS devices accomplish record values for BVdss*ft > 900 VGHz. (5) Both, HV-NLDMOS and HV-PLDMOS meet the requirement for low hot carrier induced device degradation of Idlin and Idsat < 10% in 20 years at Vdd = ±42 V.

ACKNOWLEDGEMENT

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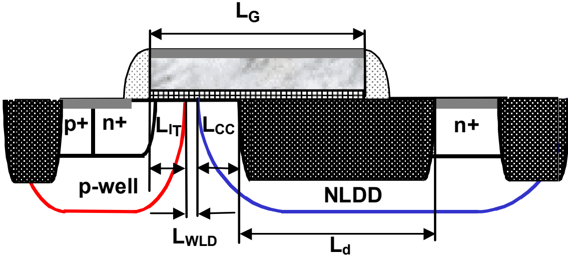

Fig. 1. Schematic cross section of HV-NLDMOS Transistor.

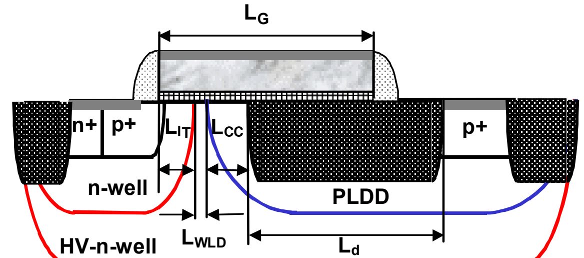

Fig. 2. Schematic cross section of HV-PLDMOS Transistor with deep HV-n-well.

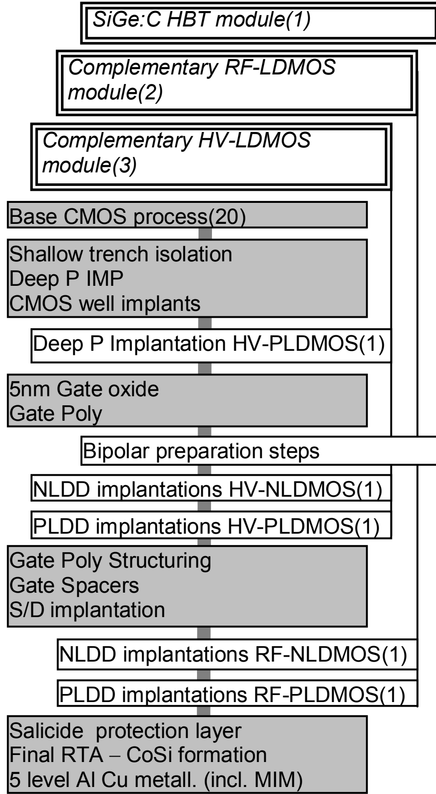

Fig. 3. Modular device integration into base RF BiCMOS process flow. The numbers in brackets indicate the corresponding mask steps.

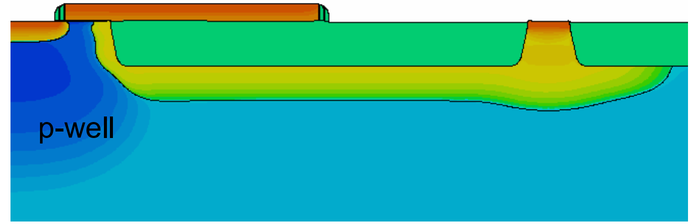

Fig. 4. Simulated doping distribution for HV-NLDMOS Transistor.

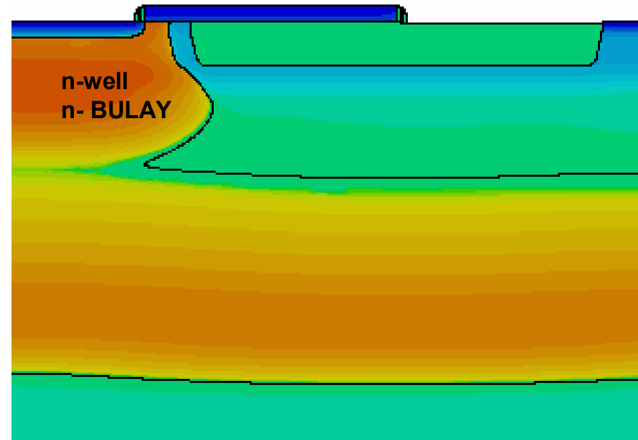

Fig. 5. Simulated doping distribution for HV-PLDMOS Transistor with deep HV-n-well.

	Ld [µm]	Ron [Ω mm]	Ron [m Ω mm^2]	Idsat [µA/µm]	BVds [V]	ft@Vd 20V [GHz]	fmax@Vd20V [GHz]
NLDMOS	1	7.3	22.7	518	40	13.1	39
	2	9.0	37.2	459	62	11.9	36.9
	3	11.7	59.7	370	83	10.9	41
	5	15.6	110.7	345	92	9.8	31.7
	8	23.3	236.0	314	103	9	29.4
PLDMOS	1	24.3	75.8	180	-47		
	2	31.1	128.0	173	-55		
	3	40.0	204.6	163	-71		
	5	52.8	375.9	150	-73	2.7	8.6
	8	70.9	717.0	136	-74		

Table 1. Electrical device parameters for PLDMOS and NLDMOS as function of drift length Ld.

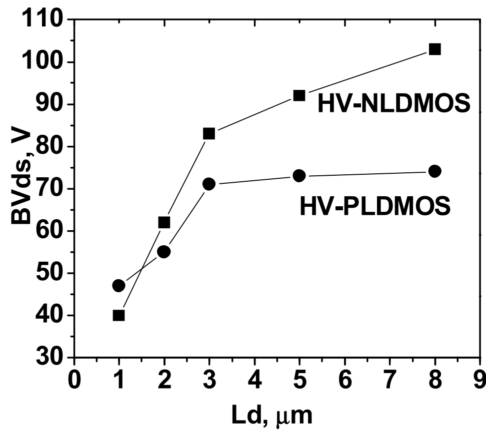

Fig. 6. BVdss as function of drift length Ld. Saturation of BVdss for PLDMOS due to onset of vertical break down.

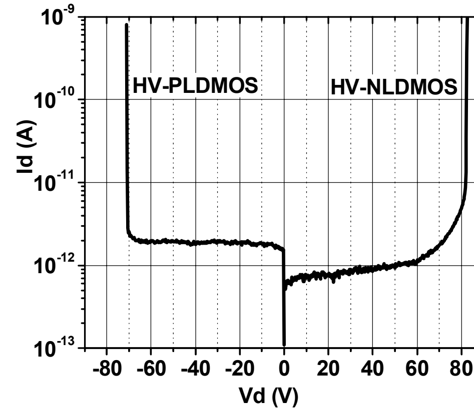

Fig. 7. Break down characteristics of PLDMOS and NLDMOS (w = 5.6 μm, Ld = 3 μm).

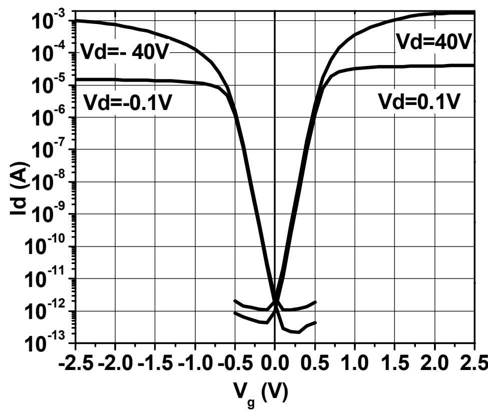

Fig. 8. Transfer characteristics in linear and saturation operation mode for PLDMOS and NLDMOS (w = 5.6 μm, Ld = 3μm).

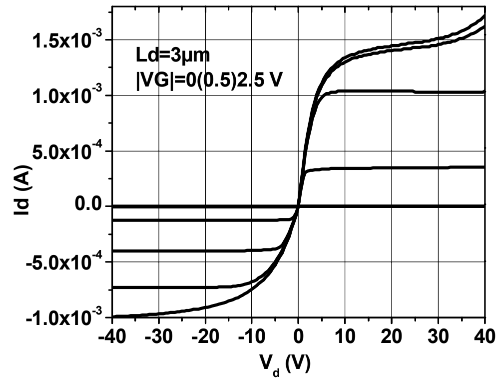

Fig. 9. Output characteristics for PLDMOS and NLDMOS (w = 5.6 μm, Ld = 3 μm).

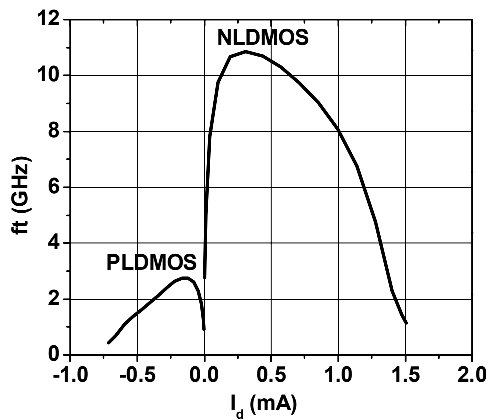

Fig. 10. Measured ft as function of Vg @ |Vd|=20V (w = 5.6 μm, Ld = 3μm for NLDMOS, w = 5.6 μm, Ld = 5μm for PLDMOS).

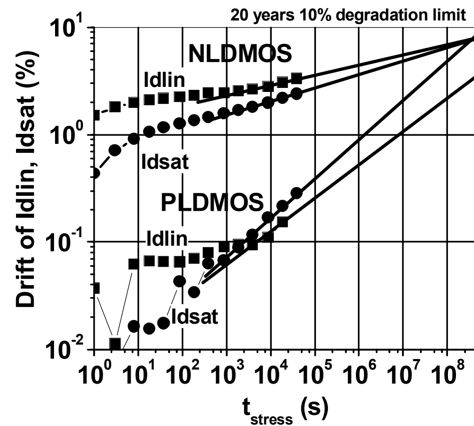

Fig. 11. Drift stability of PLDMOS and NLDMOS (Vd,stress = 42 V).